What is claimed is:

1. A semiconductor integrated circuit, comprising:

a memory, which has a set of redundant lines for repair in a Column direction;

a test pattern generating section, which generates a specific test pattern for said memory;

a comparing section, which reads an output from said memory to judge whether a faulty cell exists in said memory or not, and outputs a signal showing the existence or nonexistence of said faulty cell, and including a pass/fail judgment signal for every bit;

a first data storage section, which during an test of said memory, retrieves a signal which has branched from all or a part of Column address signals which are inputted into said memory from said test pattern generating section, and the pass/fail judgment signal for every said bit generated by said comparing section as faulty address data, and during an test of a peripheral logic of said memory, forms a part of a scan chain, and is used for observing an input signal into said memory;

a second data storage section, which receives an output signal of said comparing section to store a state of the presence or absence of a failure corresponding to the existence or nonexistence of said faulty cell; and

a repair judging section, which receives an input to said first data storage section and an output of retained contents

in said first data storage section, and judges that said memory is repairable,

wherein when said second data storage section is in a state where said failure exists, said first data storage section holds the data retained in said first data storage section.

2. The semiconductor integrated circuit according to Claim 1, wherein said first data storage section has a selector which can selectively retrieve a data input signal inputted into said memory from said test pattern generating section, or a pass/fail judgment signal for said every bit.

3. The semiconductor integrated circuit according to Claim 1, wherein when receiving a judgment of a failure with a plurality bit faults as the pass/fail judgment signal for every bit generated by said comparing section, said repair judging section judges that said memory is not repairable.

4. A semiconductor integrated circuit, comprising:

a memory, which has a set of redundant lines for repair in a Column direction;

a test pattern generating section, which generates a specific test pattern for said memory;

a comparing section, which reads an output from said memory to judge whether a faulty cell exists in said memory or not, and outputs a signal showing the existence or nonexistence of said faulty cell, and including a pass/fail judgment signal for every bit;

a first data storage section, which during an test of said memory, retrieves a signal which has branched from all or a part of Column address signals which are inputted into said memory from said test pattern generating section, and the pass/fail judgment signal for every said bit generated by said comparing section as faulty address data, and during an test of a peripheral logic of said memory, forms a part of a scan chain, and is used for observing an input signal into said memory; and

a repair judging section, which receives an input to said first data storage section and an output of retained contents in said first data storage section, and judges that said memory is repairable,

wherein said first data storage section receives a FAIL signal which is outputted from said comparing section, and when a faulty cell exists in said memory, becomes active and maintains in an active state until the test is completed, and when said FAIL signal is active, holds the data retained in said first data storage section.

5. The semiconductor integrated circuit according to Claim 4, wherein said first data storage section has a selector which can selectively retrieve a data input signal inputted into said memory from said test pattern generating section, or a pass/fail judgment signal for said every bit.

6. The semiconductor integrated circuit according to Claim 4, wherein when receiving a judgment of a failure with

a plurality of bit faults as the pass/fail judgment signal for every bit generated by said comparing section, said repair judging section judges that said memory is not repairable.

7. A semiconductor integrated circuit, comprising:

a memory, which has a pair of redundant lines for repair in a Row direction;

a test pattern generating section, which generates a specific test pattern for said memory;

a comparing section, which reads an output from said memory to judge whether a fault cell exists in said memory or not, and outputs a signal which shows the existence or nonexistence of said faulty cell;

a first data storage section, which during an test of said memory, retrieves all Row address signals or a signal which has branched a part of bits therefrom inputted into said memory from said test pattern generating section as faulty address data, and during an test of a peripheral logic of said memory, is used for observing the input signal into said memory as a part of the scan chain;

a second data storage section, which receives an output signal of said comparing section to store a state of the presence or absence of a failure corresponding to the existence or nonexistence of said faulty cell; and

a repair judging section, which receives an input to said first data storage section and an output of retained contents

in said first data storage section, and judges that said memory is repairable,

wherein when said second data storage section is in a state where said failure exists, said first data storage section holds the data retained in said first data storage section.

8. A semiconductor integrated circuit, comprising:

a memory, which has a pair of redundant lines for repair in a Row direction;

a test pattern generating section, which generates a specific test pattern for said memory;

a comparing section, which reads an output from said memory to judge whether a fault cell exists in said memory or not, and outputs a signal which shows the existence or nonexistence of said faulty cell;

a first data storage section, which during an test of said memory retrieves all Row address signals or a signal which has branched a part of bits therefrom inputted into said memory from said test pattern generating section as faulty address data, and during an test of a peripheral logic of said memory, is used for observing the input signal into said memory as a part of the scan chain; and

a repair judging section, which receives an input to said first data storage section and an output of retained contents in said first data storage section, and judges that said memory is repairable,

wherein said first data storage section receives a FAIL signal which is outputted from said comparing section, and when a faulty cell exists in said memory, becomes active and maintains in an active state until the test is completed, and when said FAIL signal is active, holds the data retained in said first data storage section.

9. A semiconductor integrated circuit, comprising:

a memory, which has redundant lines for repair in a Column direction and a Row direction,

a test pattern generating section, which generates a specific test pattern for said memory;

a comparing section, which reads an output from said memory to judge whether a fault cell exists in said memory or not, and outputs a signal which shows the existence or nonexistence of said faulty cell;

a first data storage section, which during an test of said memory, retrieves a signal which has been branched from an address signal inputted into said memory from said test pattern generating section, and an output signal from said comparing section as faulty address data, and during an test of a peripheral logic of said memory, is used for observing the input signal into said memory as a part of the scan chain;

a second data storage section, which receives an output signal of said comparing section to store a state of the presence or absence of a failure corresponding to the existence or

nonexistence of said faulty cell; and

a repair judging section, which receives an input to said first data storage section and an output of retained contents in said first data storage section, and judges that said memory is repairable,

wherein when said second data storage section is in a state where said failure exists, said first data storage section holds the data retained in said first data storage section.

10. The semiconductor integrated circuit according to any one of claims 1-9, wherein when a MONITOR signal, which is a signal outputted from said comparing section and becomes active only when a faulty cell exists in said memory, and a FAIL signal, which becomes active when a faulty cell exists in said memory and keeps in the active state until the test is completed are active, said repair judging section compares an input of said first data storage section with an output of said first data storage section to judges whether or not said memory is repairable.

11. An test method of the semiconductor integrated circuit according to any one of claims 1-9, wherein the test method of the semiconductor integrated circuit characterized in that the first data storage section is used for retaining fault information on the memory when inspecting the memory, and is used for observing an input signal into the memory when inspecting the peripheral logic of the memory.